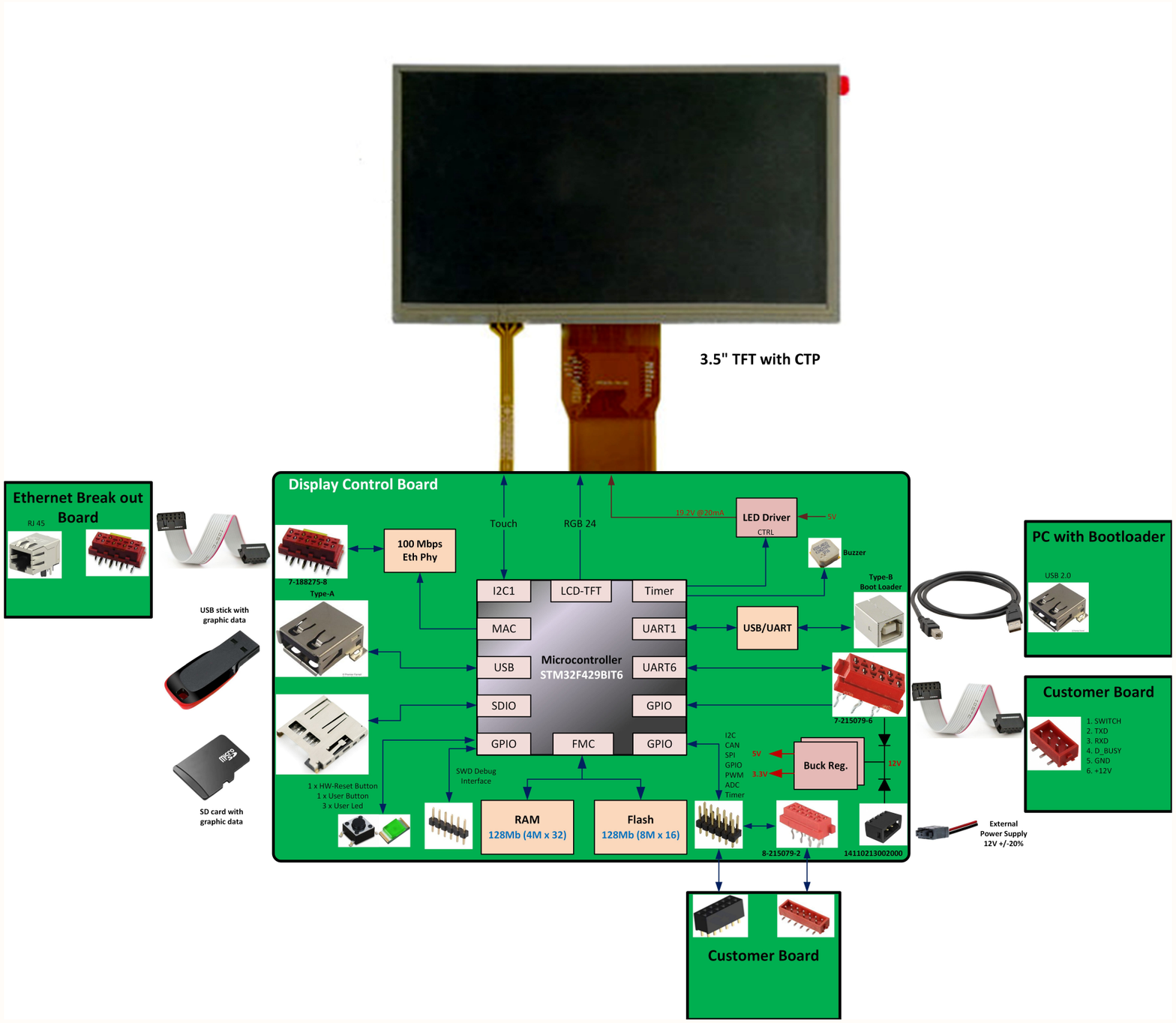
COVER PAGE

DS18_SYSG_DISP_1116

DISPLAY CONTROL BOARD

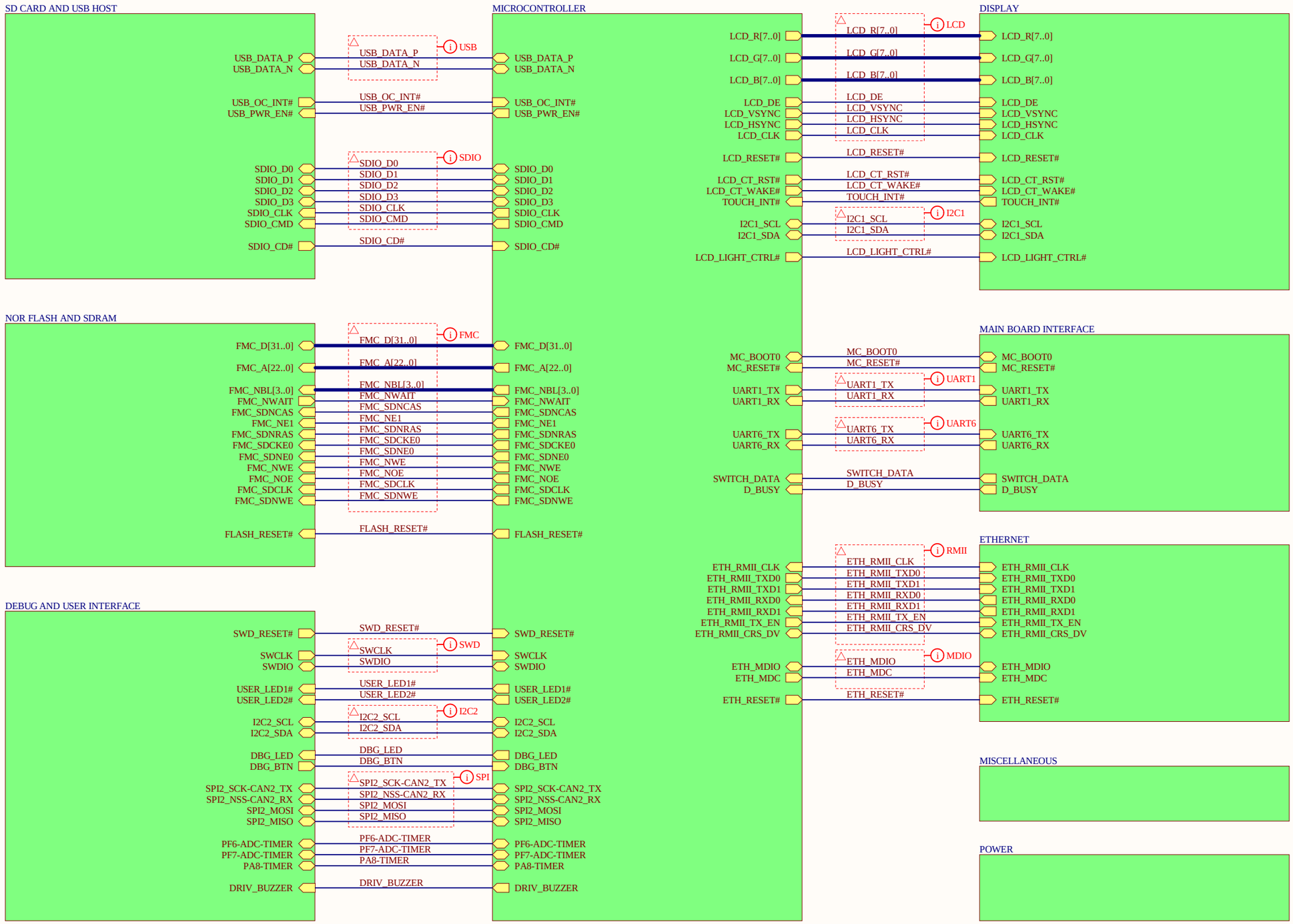
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_V200.PrjPcb			
Document:	P01_COVER_PAGE.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	1

BLOCK DIAGRAM



Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P02_Block_Diagram.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	2

TOP LEVEL PAGE



Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P03_TOP_LEVEL_PAGE.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	3

MICROCONTROLLER A-E

FMC_A[22..0]
FMC_D[31..0]
FMC_NBL[3..0]

Boot mode selection pins		Boot mode
BOOT1	BOOT0	
X	0	Main Flash memory
0	1	System memory
1	1	Embedded SRAM

VCC_3V3
R1 10k/100mW/50V/±1%
R2 10k/100mW/50V/±1%
GND

IC1A
STM32F429BIT6

DRIV_BUZZER	DRIV_BUZZER	43	PA0/TIM2_CH1/TIM2_ETR/TIM5_CH1/TIM8_ETR/USART2_CTS/UART4_TX/ETH_MII_CRS/EVENTOUT/ADC123_IN0/WKUP
ETH_RMII_CLK	ETH_RMII_CLK	44	PA1/TIM2_CH2/TIM5_CH2/USART2_RTS/UART4_RX/ETH_MII_RX_CLK/ETH_RMII_REF_CLK/EVENTOUT/ADC123_IN1
ETH_MDIO	ETH_MDIO	45	PA2/TIM2_CH3/TIM5_CH3/TIM9_CH1/USART2_TX/ETH_MDIO/EVENTOUT/ADC123_IN2
LCD_CT_WAKE#	LCD_CT_WAKE#	50	PA3/TIM2_CH4/TIM5_CH4/TIM9_CH2/USART2_RX/OTG_HS_ULPI_D0/ETH_MII_COL/LCD_B5/EVENTOUT/ADC123_IN3
LCD_CT_RST#	LCD_CT_RST#	53	PA4/SPI1_NSS/SPI3_NSS/I2S3_WS/USART2_CK/OTG_HS_SOF/DCMI_HSYNC/LCD_VSYNC/EVENTOUT/ADC12_IN4/DAC_OUT1
USER_LED2#	USER_LED2#	54	PA5/TIM2_CH1/TIM2_ETR/TIM8_CH1N/SPI1_SCK/OTG_HS_ULPI_CK/EVENTOUT/ADC12_IN5/DAC_OUT2
USER_LED1#	USER_LED1#	55	PA6/TIM1_BKIN/TIM3_CH1/TIM8_BKIN/SPI1_MISO/TIM13_CH1/DCMI_PIXCLK/LCD_G2/EVENTOUT/ADC12_IN6
ETH_RMII_CRS_DV	ETH_RMII_CRS_DV	56	PA7/TIM1_CH1N/TIM3_CH2/TIM8_CH1N/SPI1_MOSI/TIM14_CH1/ETH_MII_RX_DV/ETH_RMII_CRS_DV/EVENTOUT/ADC12_IN7
PA8-TIMER	PA8-TIMER	142	PA8/MCO1/TIM1_CH1/I2C3_SCL/USART1_CK/OTG_FS_SOF/LCD_R6/EVENTOUT
UART1_TX	UART1_TX	143	PA9/TIM1_CH2/I2C3_SMBA/USART1_TX/DCMI_D0/EVENTOUT/OTG_FS_VBUS
UART1_RX	UART1_RX	144	PA10/TIM1_CH3/USART1_RX/OTG_FS_ID/DCMI_D1/EVENTOUT
USB_DATA_N	USB_DATA_N	145	PA11/TIM1_CH4/USART1_CTS/CAN1_RX/LCD_R4/OTG_FS_DM/EVENTOUT
USB_DATA_P	USB_DATA_P	146	PA12/TIM1_ETR/USART1_RTS/CAN1_TX/LCD_R5/OTG_FS_DP/EVENTOUT
SWDIO	SWDIO	147	PA13/JTMS-SWDIO/EVENTOUT
SWCLK	SWCLK	159	PA14/JTCK-SWCLK/EVENTOUT
	JTAG_JTDI	160	PA15/JTDI/TIM2_CH1/TIM2_ETR/SPI1_NSS/SPI3_NSS/I2S3_WS/EVENTOUT

tp94 SWDIO
tp95 SWCLK
tp96

IC1B
STM32F429BIT6

SWITCH_DATA	SWITCH_DATA	61	PB0/TIM1_CH2N/TIM3_CH3/TIM8_CH2N/LCD_R3/OTG_HS_ULPI_D1/ETH_MII_RXD2/EVENTOUT/ADC12_IN8
D_BUSY	D_BUSY	62	PB1/TIM1_CH3N/TIM3_CH4/TIM8_CH3N/LCD_R6/OTG_HS_ULPI_D2/ETH_MII_RXD3/EVENTOUT/ADC12_IN9
	BOOT1	63	PB2/EVENTOUT/BOOT1
tp97	JTDO	192	PB3/JTDO/TRACESWO/TIM2_CH2/SPI1_SCK/SPI3_SCK/I2S3_CK/EVENTOUT
tp98	NJTRST	193	PB4/NJTRST/TIM3_CH1/SPI1_MISO/SPI3_MISO/I2S3ext_SD/EVENTOUT
USB_PWR_EN#	USB_PWR_EN#	194	PB5/TIM3_CH2/I2C1_SMBA/SPI1_MOSI/SPI3_MOSI/I2S3_SD/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_OUT/FMC_SDCKE1/DCMI_D10/EVENTOUT
I2C1_SCL	I2C1_SCL	195	PB6/TIM4_CH1/I2C1_SCL/USART1_TX/CAN2_TX/FMC_SDNE1/DCMI_D5/EVENTOUT
I2C1_SDA	I2C1_SDA	196	PB7/TIM4_CH2/I2C1_SDA/USART1_RX/FMC_NL/DCMI_VSYNC/EVENTOUT
USB_OC_INT#	USB_OC_INT#	198	PB8/TIM4_CH3/TIM10_CH1/I2C1_SCL/CAN1_RX/ETH_MII_TXD3/SDIO_D4/DCMI_D6/LCD_B6/EVENTOUT
ETH_RESET#	ETH_RESET#	199	PB9/TIM4_CH4/TIM11_CH1/I2C1_SDA/SPI2_NSS/I2S2_WS/CAN1_TX/SDIO_D5/DCMI_D7/LCD_B7/EVENTOUT
I2C2_SCL	I2C2_SCL	90	PB10/TIM2_CH3/I2C2_SCL/SPI2_SCK/I2S2_CK/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER/LCD_G4/EVENTOUT
I2C2_SDA	I2C2_SDA	91	PB11/TIM2_CH4/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_MII_TX_EN/ETH_RMII_TX_EN/LCD_G5/EVENTOUT
SPI2_NSS-CAN2_RX	SPI2_NSS-CAN2_RX	104	PB12/TIM1_BKIN/I2C2_SMBA/SPI2_NSS/I2S2_WS/USART3_CK/CAN2_RX/OTG_HS_ULPI_D5/ETH_MII_TXD0/ETH_RMII_TXD0/OTG_HS_ID/EVENTOUT
SPI2_SCK-CAN2_TX	SPI2_SCK-CAN2_TX	105	PB13/TIM1_CH1N/SPI2_SCK/I2S2_CK/USART3_CTS/CAN2_TX/OTG_HS_ULPI_D6/ETH_MII_TXD1/ETH_RMII_TXD1/EVENTOUT/OTG_HS_VBUS
SPI2_MISO	SPI2_MISO	106	PB14/TIM1_CH2N/TIM8_CH2N/SPI2_MISO/I2S2ext_SD/USART3_RTS/TIM12_CH1/OTG_HS_DM/EVENTOUT
SPI2_MOSI	SPI2_MOSI	107	PB15/RTC_REFIN/TIM1_CH3N/TIM8_CH3N/SPI2_MOSI/I2S2_SD/TIM12_CH2/OTG_HS_DP/EVENTOUT

IC1C
STM32F429BIT6

		35	PC0/OTG_HS_ULPI_STP/FMC_SDNWE/EVENTOUT/ADC123_IN10
ETH_MDC	ETH_MDC	36	PC1/ETH_MDC/EVENTOUT/ADC123_IN11
		37	PC2/SPI2_MISO/I2S2ext_SD/OTG_HS_ULPI_DIR/ETH_MII_TXD2/FMC_SDNE0/EVENTOUT/ADC123_IN12
		38	PC3/SPI2_MOSI/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CLK/FMC_SDCKE0/EVENTOUT/ADC123_IN13
ETH_RMII_RXD0	ETH_RMII_RXD0	57	PC4/ETH_MII_RXD0/ETH_RMII_RXD0/EVENTOUT/ADC12_IN14
ETH_RMII_RXD1	ETH_RMII_RXD1	58	PC5/ETH_MII_RXD1/ETH_RMII_RXD1/EVENTOUT/ADC12_IN15
UART6_TX	UART6_TX	138	PC6/TIM3_CH1/TIM8_CH1/I2S2_MCK/USART6_TX/SDIO_D6/DCMI_D0/LCD_HSYNC/EVENTOUT
UART6_RX	UART6_RX	139	PC7/TIM3_CH2/TIM8_CH2/I2S3_MCK/USART6_RX/SDIO_D7/DCMI_D1/LCD_G6/EVENTOUT
SDIO_D0	SDIO_D0	140	PC8/TIM3_CH3/TIM8_CH3/USART6_CK/SDIO_D0/DCMI_D2/EVENTOUT
SDIO_D1	SDIO_D1	141	PC9/MCO2/TIM3_CH4/TIM8_CH4/I2C3_SDA/I2S_CKIN/SDIO_D1/DCMI_D3/EVENTOUT
SDIO_D2	SDIO_D2	161	PC10/SPI3_SCK/I2S3_CK/USART3_TX/UART4_TX/SDIO_D2/DCMI_D8/LCD_R2/EVENTOUT
SDIO_D3	SDIO_D3	162	PC11/I2S3ext_SD/SPI3_MISO/USART3_RX/UART4_RX/SDIO_D3/DCMI_D4/EVENTOUT
SDIO_CLK	SDIO_CLK	163	PC12/SPI3_MOSI/I2S3_SD/USART3_CK/UART5_TX/SDIO_CK/DCMI_D9/EVENTOUT
DBG_BTN	DBG_BTN	8	PC13/EVENTOUT/TAMP_1
	OSC32_IN	9	PC14/EVENTOUT/OSC32_IN
	OSC32_OUT	10	PC15/EVENTOUT/OSC32_OUT

R3 27R/100mW/50V/±1%
Q1 32.768kHz/4pF/20ppm
tp1 tp2
R4 1Meg/100mW/50V/±1%
C1 6p8/50V/±0.25pF, NP0
ST_OSC32
C2 6p8/50V/±0.25pF, NP0
GND GND

IC1D
STM32F429BIT6

	FMC_D2	164	PD0/CAN1_RX/FMC_D2/EVENTOUT
	FMC_D3	165	PD1/CAN1_TX/FMC_D3/EVENTOUT
SDIO_CMD	SDIO_CMD	166	PD2/TIM3_ETR/UART5_RX/SDIO_CMD/DCMI_D11/EVENTOUT
TOUCH_INT#	TOUCH_INT#	167	PD3/SPI2_SCK/I2S2_CK/USART2_CTS/FMC_CLK/DCMI_D5/LCD_G7/EVENTOUT
FMC_NOE	FMC_NOE	168	PD4/USART2_RTS/FMC_NOE/EVENTOUT
FMC_NWE	FMC_NWE	169	PD5/USART2_TX/FMC_NWE/EVENTOUT
FMC_NWAIT	FMC_NWAIT	172	PD6/SPI3_MOSI/I2S3_SD/SAI1_SD_A/USART2_RX/FMC_NWAIT/DCMI_D10/LCD_B2/EVENTOUT
FMC_NE1	FMC_NE1	173	PD7/USART2_CK/FMC_NE1/FMC_NCE2/EVENTOUT
	FMC_D13	108	PD8/USART3_TX/FMC_D13/EVENTOUT
	FMC_D14	109	PD9/USART3_RX/FMC_D14/EVENTOUT
	FMC_D15	110	PD10/USART3_CK/FMC_D15/LCD_B3/EVENTOUT
	FMC_A16	111	PD11/USART3_CTS/FMC_A16/EVENTOUT
	FMC_A17	112	PD12/TIM4_CH1/USART3_RTS/FMC_A17/EVENTOUT
	FMC_A18	113	PD13/TIM4_CH2/FMC_A18/EVENTOUT
	FMC_D0	116	PD14/TIM4_CH3/FMC_D0/EVENTOUT
	FMC_D1	117	PD15/TIM4_CH4/FMC_D1/EVENTOUT

IC1E
STM32F429BIT6

	FMC_NBL0	200	PE0/TIM4_ETR/UART8_RX/FMC_NBL0/DCMI_D2/EVENTOUT
	FMC_NBL1	201	PE1/UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT
		1	PE2/TRACECLK/SPI4_SCK/SAI1_MCLK_A/ETH_MII_TXD3/FMC_A23/EVENTOUT
FMC_A19	FMC_A19	2	PE3/TRACED0/SAI1_SD_B/FMC_A19/EVENTOUT
FMC_A20	FMC_A20	3	PE4/TRACED1/SPI4_NSS/SAI1_FS_A/FMC_A20/DCMI_D4/LCD_B0/EVENTOUT
FMC_A21	FMC_A21	4	PE5/TRACED2/TIM9_CH1/SPI4_MISO/SAI1_SCK_A/FMC_A21/DCMI_D6/LCD_G0/EVENTOUT
FMC_A22	FMC_A22	5	PE6/TRACED3/TIM9_CH2/SPI4_MOSI/SAI1_SD_A/FMC_A22/DCMI_D7/LCD_G1/EVENTOUT
FMC_D4	FMC_D4	79	PE7/TIM1_ETR/UART7_Rx/FMC_D4/EVENTOUT
FMC_D5	FMC_D5	80	PE8/TIM1_CH1N/UART7_Tx/FMC_D5/EVENTOUT
FMC_D6	FMC_D6	81	PE9/TIM1_CH1/FMC_D6/EVENTOUT
FMC_D7	FMC_D7	84	PE10/TIM1_CH2N/FMC_D7/EVENTOUT
FMC_D8	FMC_D8	85	PE11/TIM1_CH2/SPI4_NSS/FMC_D8/LCD_G3/EVENTOUT
FMC_D9	FMC_D9	86	PE12/TIM1_CH3N/SPI4_SCK/FMC_D9/LCD_B4/EVENTOUT
FMC_D10	FMC_D10	87	PE13/TIM1_CH3/SPI4_MISO/FMC_D10/LCD_DE/EVENTOUT
FMC_D11	FMC_D11	88	PE14/TIM1_CH4/SPI4_MOSI/FMC_D11/LCD_CLK/EVENTOUT
FMC_D12	FMC_D12	89	PE15/TIM1_BKIN/FMC_D12/LCD_R7/EVENTOUT

Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P04_Microcontroller_A-E.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	4

MICROCONTROLLER F-K

LCD_R[7..0] — LCD_R[7..0]
LCD_G[7..0] — LCD_G[7..0]
LCD_B[7..0] — LCD_B[7..0]

FMC_A[22..0] — FMC_A[22..0]
FMC_D[31..0] — FMC_D[31..0]
FMC_NBL[3..0] — FMC_NBL[3..0]

IC1F
STM32F429BIT6

FMC_A0	16	PF0/I2C2_SDA/FMC_A0/EVENTOUT
FMC_A1	17	PF1/I2C2_SCL/FMC_A1/EVENTOUT
FMC_A2	18	PF2/I2C2_SMBA/FMC_A2/EVENTOUT
FMC_A3	22	PF3/FMC_A3/EVENTOUT/ADC3_IN9
FMC_A4	23	PF4/FMC_A4/EVENTOUT/ADC3_IN14
FMC_A5	24	PF5/FMC_A5/EVENTOUT/ADC3_IN15
PF6-ADC-TIMER	27	PF6/TIM10_CH1/SPI5_NSS/SAI1_SD_B/UART7_Rx/FMC_NIORD/EVENTOUT/ADC3_IN4
PF7-ADC-TIMER	28	PF7/TIM11_CH1/SPI5_SCK/SAI1_MCLK_B/UART7_Tx/FMC_NREG/EVENTOUT/ADC3_IN5
	29	PF8/SPI5_MISO/SAI1_SCK_B/TIM13_CH1/FMC_NIOWR/EVENTOUT/ADC3_IN6
	30	PF9/SPI5_MOSI/SAI1_FS_B/TIM14_CH1/ FMC_CD/EVENTOUT/ADC3_IN7
	31	PF10/FMC_INTR/DCMI_D11/LCD_DE/EVENTOUT/ADC3_IN8
FMC_SDNRAS	70	PF11/SPI5_MOSI/FMC_SDNRAS/DCMI_D12/EVENTOUT
FMC_A6	71	PF12/FMC_A6/EVENTOUT
FMC_A7	74	PF13/FMC_A7/EVENTOUT
FMC_A8	75	PF14/FMC_A8/EVENTOUT
FMC_A9	76	PF15/FMC_A9/EVENTOUT

IC1J
STM32F429BIT6

LCD_R1	65	PJ0/LCD_R1/EVENTOUT
LCD_R2	66	PJ1/LCD_R2/EVENTOUT
LCD_R3	67	PJ2/LCD_R3/EVENTOUT
LCD_R4	68	PJ3/LCD_R4/EVENTOUT
LCD_R5	69	PJ4/LCD_R5/EVENTOUT
LCD_R6	95	PJ5/LCD_R6/EVENTOUT
LCD_R7	118	PJ6/LCD_R7/EVENTOUT
LCD_G0	119	PJ7/LCD_G0/EVENTOUT
LCD_G1	120	PJ8/LCD_G1/EVENTOUT
LCD_G2	121	PJ9/LCD_G2/EVENTOUT
LCD_G3	122	PJ10/LCD_G3/EVENTOUT
LCD_G4	123	PJ11/LCD_G4/EVENTOUT
LCD_B0	174	PJ12/LCD_B0/EVENTOUT
LCD_B1	175	PJ13/LCD_B1/EVENTOUT
LCD_B2	176	PJ14/LCD_B2/EVENTOUT
LCD_B3	177	PJ15/LCD_B3/EVENTOUT

IC1G
STM32F429BIT6

FMC_A10	77	PG0/FMC_A10/EVENTOUT
FMC_A11	78	PG1/FMC_A11/EVENTOUT
FMC_A12	129	PG2/FMC_A12/EVENTOUT
FMC_A13	130	PG3/FMC_A13/EVENTOUT
FMC_A14	131	PG4/FMC_A14/FMC_BA0/EVENTOUT
FMC_A15	132	PG5/FMC_A15/FMC_BA1/EVENTOUT
	133	PG6/FMC_INT2/DCMI_D12/LCD_R7/EVENTOUT
	134	PG7/USART6_CK/FMC_INT3/DCMI_D13/LCD_CLK/EVENTOUT
FMC_SDCLK	135	PG8/SPI6_NSS/USART6_RTS/ETH_PPS_OUT/FMC_SDCLK/EVENTOUT
LCD_RESET#	179	PG9/USART6_RX/FMC_NE2/FMC_NCE3/DCMI_VSYNC/EVENTOUT
SDIO_CD#	179	PG10/LCD_G3/FMC_NCE4_1/FMC_NE3/DCMI_D2/LCD_B2/EVENTOUT
ETH_RMII_TX_EN	180	PG11/ETH_MII_TX_EN/ETH_RMII_TX_EN/FMC_NCE4_2/DCMI_D3/LCD_B3/EVENTOUT
	181	PG12/SPI6_MISO/USART6_RTS/LCD_B4/FMC_NE4/LCD_B1/EVENTOUT
ETH_RMII_TXD0	182	PG13/SPI6_SCK/USART6_CTS/ETH_MII_TXD0/ETH_RMII_TXD0/FMC_A24/EVENTOUT
ETH_RMII_TXD1	183	PG14/SPI6_MOSI/USART6_TX/ETH_MII_TXD1/ETH_RMII_TXD1/FMC_A25/EVENTOUT
FMC_SDNCAS	191	PG15/USART6_CTS/FMC_SDNCAS/DCMI_D13/EVENTOUT

IC1K
STM32F429BIT6

LCD_G5	126	PK0/LCD_G5/EVENTOUT
LCD_G6	127	PK1/LCD_G6/EVENTOUT
LCD_G7	128	PK2/LCD_G7/EVENTOUT
LCD_B4	186	PK3/LCD_B4/EVENTOUT
LCD_B5	187	PK4/LCD_B5/EVENTOUT
LCD_B6	188	PK5/LCD_B6/EVENTOUT
LCD_B7	189	PK6/LCD_B7/EVENTOUT
LCD_DE	190	PK7/LCD_DE/EVENTOUT

IC1H
STM32F429BIT6

OSC_IN	32	PH0/EVENTOUT/OSC_IN
OSC_OUT	33	PH1/EVENTOUT/OSC_OUT
FMC_SDCKE0	46	PH2/ETH_MII_CRS/FMC_SDCKE0/LCD_R0/EVENTOUT
FMC_SDNE0	47	PH3/ETH_MII_COL/FMC_SDNE0/LCD_R1/EVENTOUT
	48	PH4/I2C2_SCL/OTG_HS_ULPI_NXT/EVENTOUT
FMC_SDNWE	49	PH5/I2C2_SDA/SPI5_NSS/FMC_SDNWE/EVENTOUT
LCD_LIGHT_CTRL#	96	PH6/I2C2_SMBA/SPI5_SCK/TIM12_CH1/ETH_MII_RXD2/FMC_SDNE1/DCMI_D8/EVENTOUT
DBG_LED	97	PH7/I2C3_SCL/SPI5_MISO/ETH_MII_RXD3/FMC_SDCKE1/DCMI_D9/EVENTOUT
FMC_D16	98	PH8/I2C3_SDA/FMC_D16/DCMI_HSYNC/LCD_R2/EVENTOUT
FMC_D17	99	PH9/I2C3_SMBA/TIM12_CH2/FMC_D17/DCMI_D0/LCD_R3/EVENTOUT
FMC_D18	100	PH10/TIM5_CH1/FMC_D18/DCMI_D1/LCD_R4/EVENTOUT
FMC_D19	101	PH11/TIM5_CH2/FMC_D19/DCMI_D2/LCD_R5/EVENTOUT
FMC_D20	102	PH12/TIM5_CH3/FMC_D20/DCMI_D3/LCD_R6/EVENTOUT
FMC_D21	151	PH13/TIM8_CH1N/CAN1_TX/FMC_D21/LCD_G2/EVENTOUT
FMC_D22	152	PH14/TIM8_CH2N/FMC_D22/DCMI_D4/LCD_G3/EVENTOUT
FMC_D23	153	PH15/TIM8_CH3N/FMC_D23/DCMI_D11/LCD_G4/EVENTOUT

IC1I
STM32F429BIT6

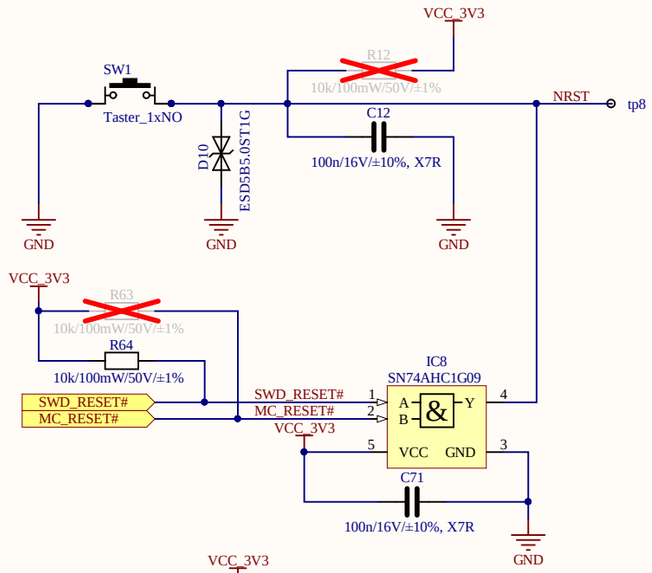
FMC_D24	154	PI0/TIM5_CH4/SPI2_NSS/I2S2_WS/FMC_D24/DCMI_D13/LCD_G5/EVENTOUT
FMC_D25	155	PI1/SPI2_SCK/I2S2_CK/FMC_D25/DCMI_D8/LCD_G6/EVENTOUT
FMC_D26	156	PI2/TIM8_CH4/SPI2_MISO/I2S2ext_SD/FMC_D26/DCMI_D9/LCD_G7/EVENTOUT
FMC_D27	157	PI3/TIM8_ETR/SPI2_MOSI/I2S2_SD/FMC_D27/DCMI_D10/EVENTOUT
FMC_NBL2	205	PI4/TIM8_BKIN/FMC_NBL2/DCMI_D5/LCD_B4/EVENTOUT
FMC_NBL3	206	PI5/TIM8_CH1/FMC_NBL3/DCMI_VSYNC/LCD_B5/EVENTOUT
FMC_D28	207	PI6/TIM8_CH2/FMC_D28/DCMI_D6/LCD_B6/EVENTOUT
FMC_D29	208	PI7/TIM8_CH3/FMC_D29/DCMI_D7/LCD_B7/EVENTOUT
	7	PI8/EVENTOUT/TAMP_2
FMC_D30	11	PI9/CAN1_RX/FMC_D30/LCD_VSYNC/EVENTOUT
FMC_D31	12	PI10/ETH_MII_RX_ER/FMC_D31/LCD_HSYNC/EVENTOUT
FLASH_RESET#	13	PI11/OTG_HS_ULPI_DIR/EVENTOUT
LCD_HSYNC	19	PI12/LCD_HSYNC/EVENTOUT
LCD_VSYNC	20	PI13/LCD_VSYNC/EVENTOUT
LCD_CLK	21	PI14/LCD_CLK/EVENTOUT
LCD_R0	64	PI15/LCD_R0/EVENTOUT

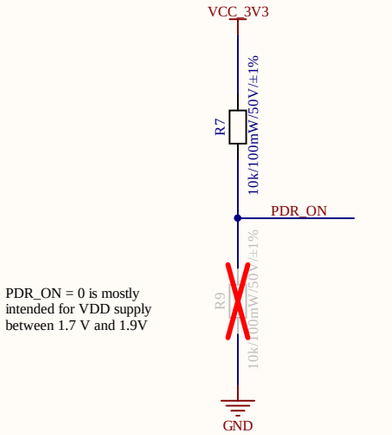
Q2
12MHz/18pF/20ppm
tp4
tp5
R5
330R/100mW/50V/±1%
R6
1Meg/100mW/50V/±1%
ST_OSC_OUT
C3
27p/50V/±5%, NP0
C4
27p/50V/±5%, NP0
GND
GND

Schematics			
Project:	Display_Control_Board_V200.PrjPcb	EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Document:	P05_Microcontroller_F-K.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	5

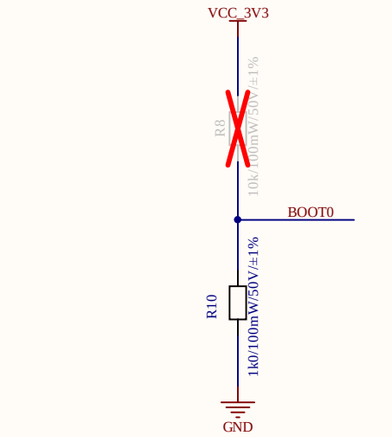
MICROCONTROLLER POWER

MicroController Reset

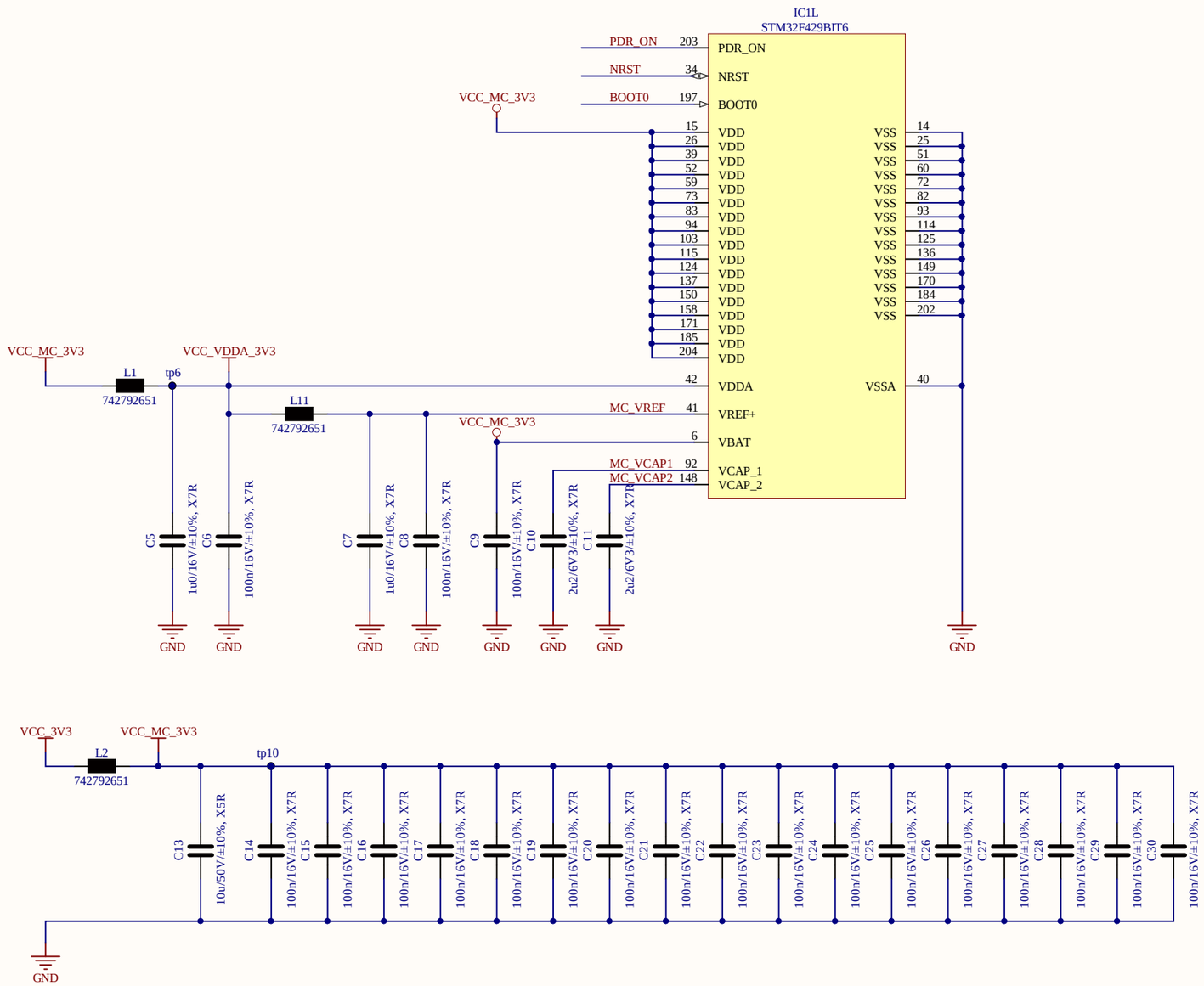




PDR_ON = 0 is mostly intended for VDD supply between 1.7 V and 1.9V



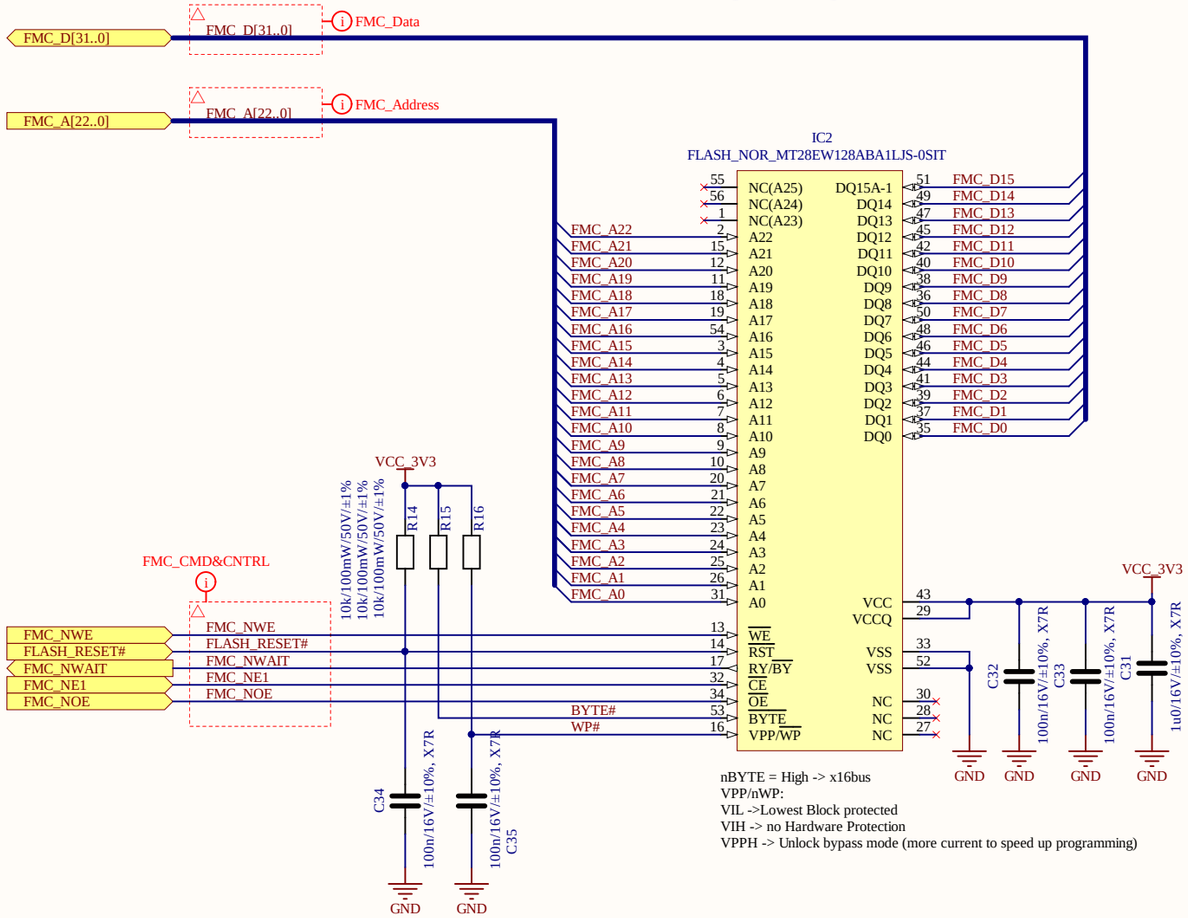
Boot mode selection pins		Boot mode
BOOT1	BOOT0	
X	0	Main Flash memory
0	1	System memory
1	1	Embedded SRAM



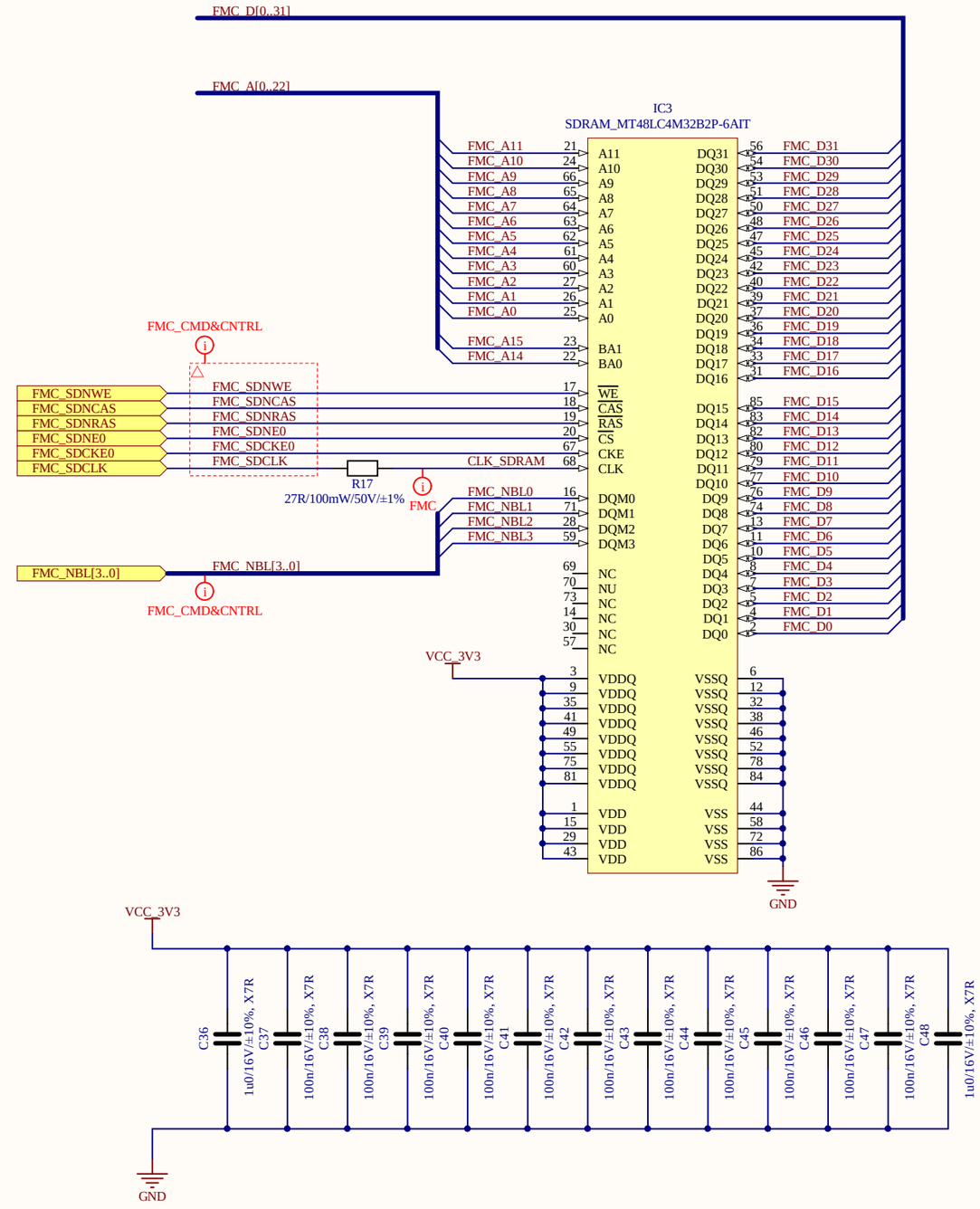
Schematics		SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P06_Microcontroller_Power.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	6

NOR FLASH AND SDRAM

NOR FLASH



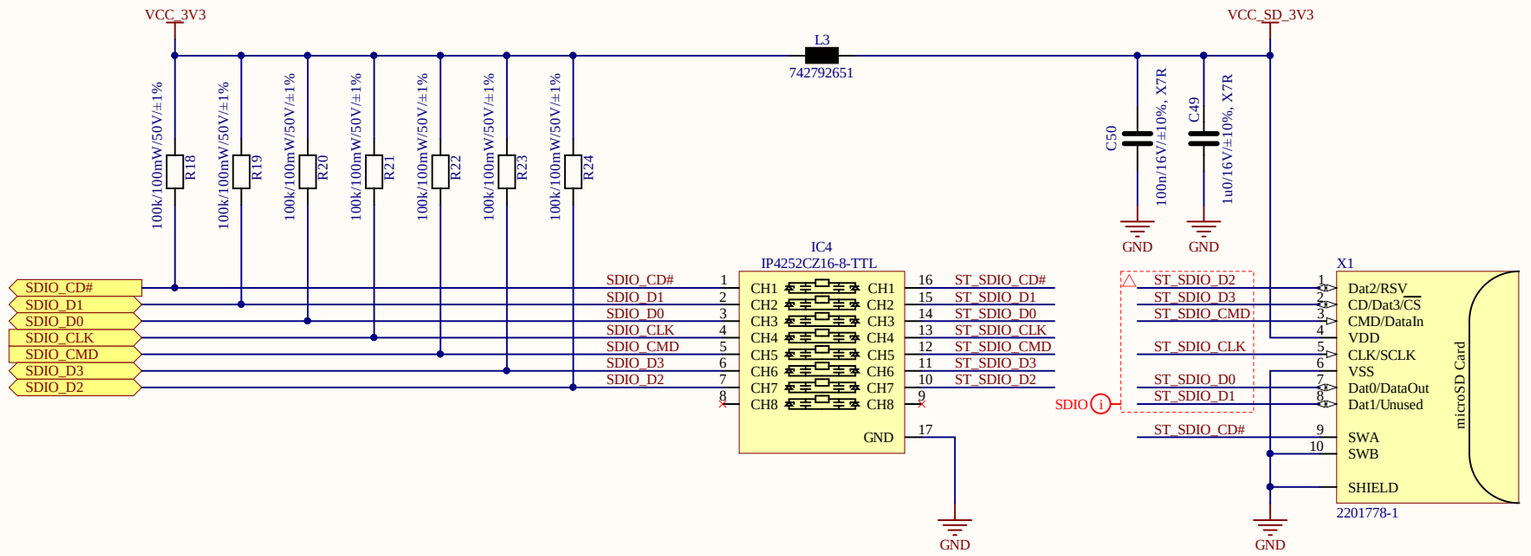
SDRAM



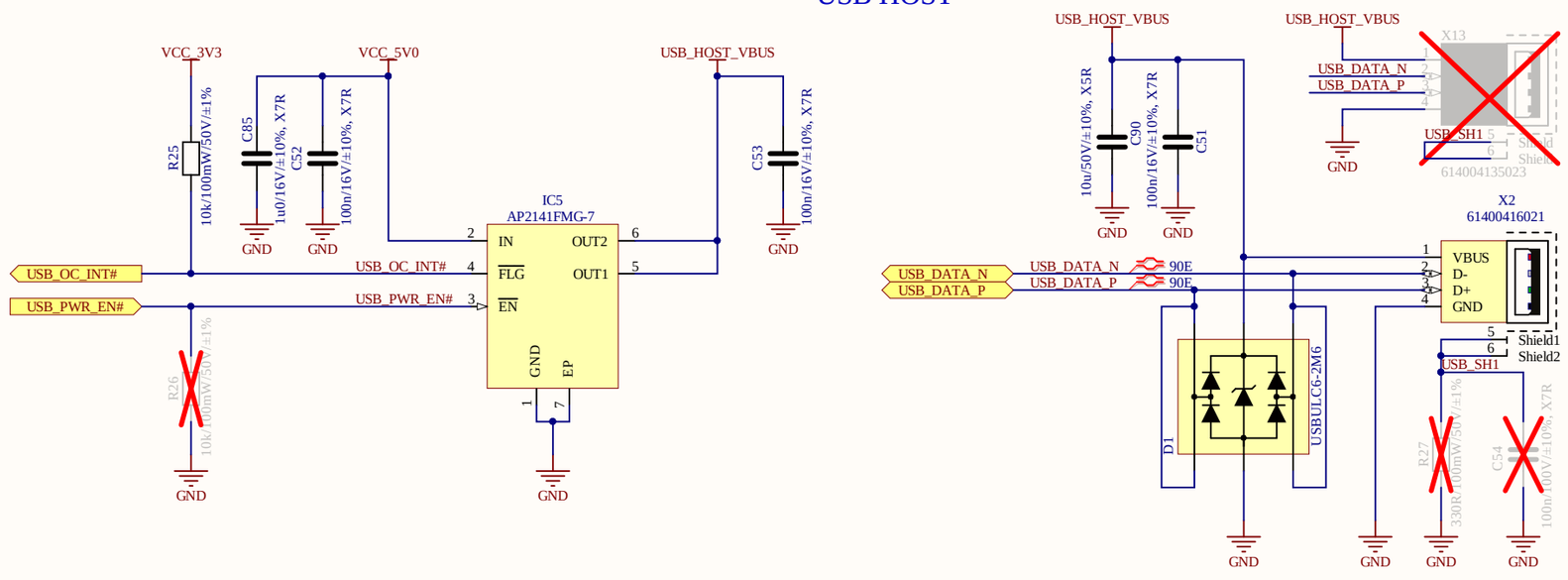
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_V200.PrjPcb			
Document:	P07_NOR_Flash_and_SDRAM.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	7

SD CARD AND USB HOST

MICRO SD CARD INTERFACE



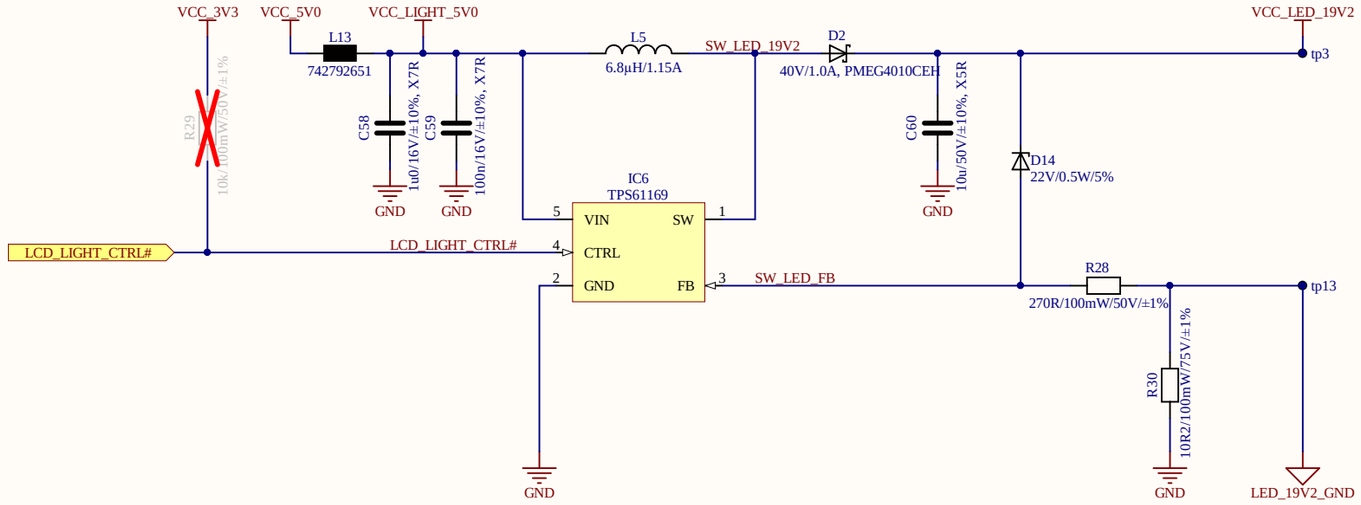
USB HOST



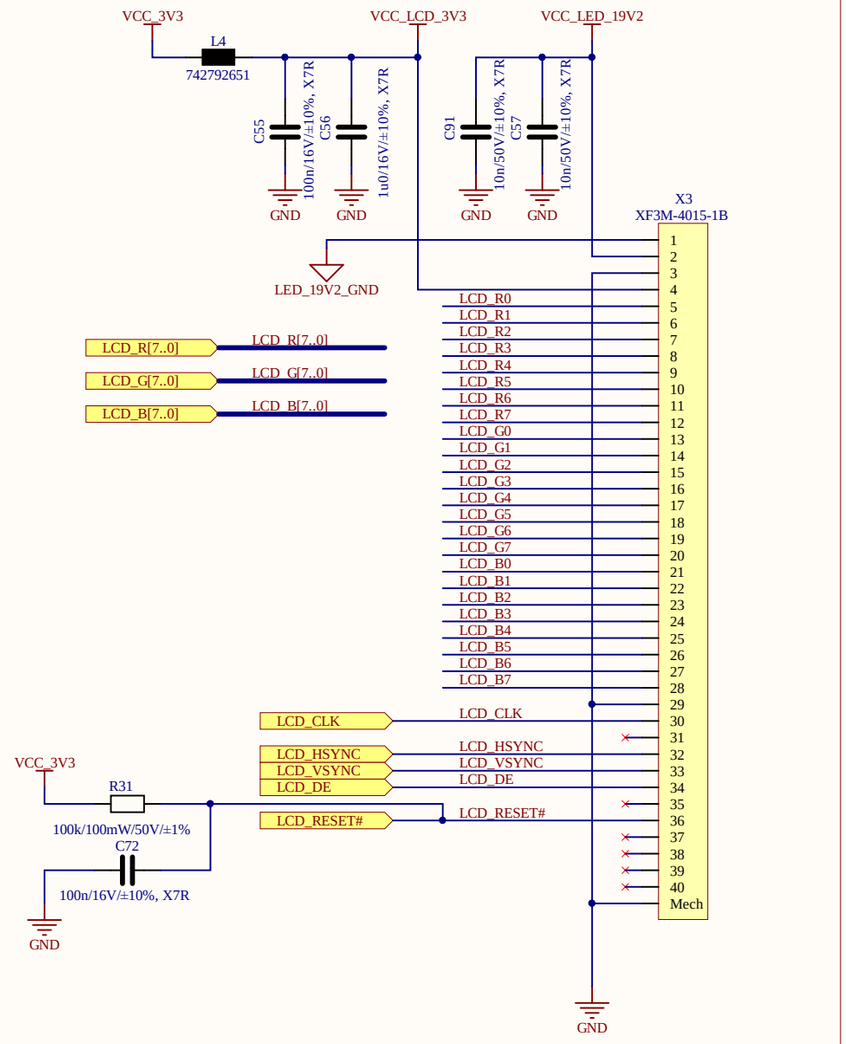
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P08_SD_Card_And_USB_Host.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	8

TFT DISPLAY

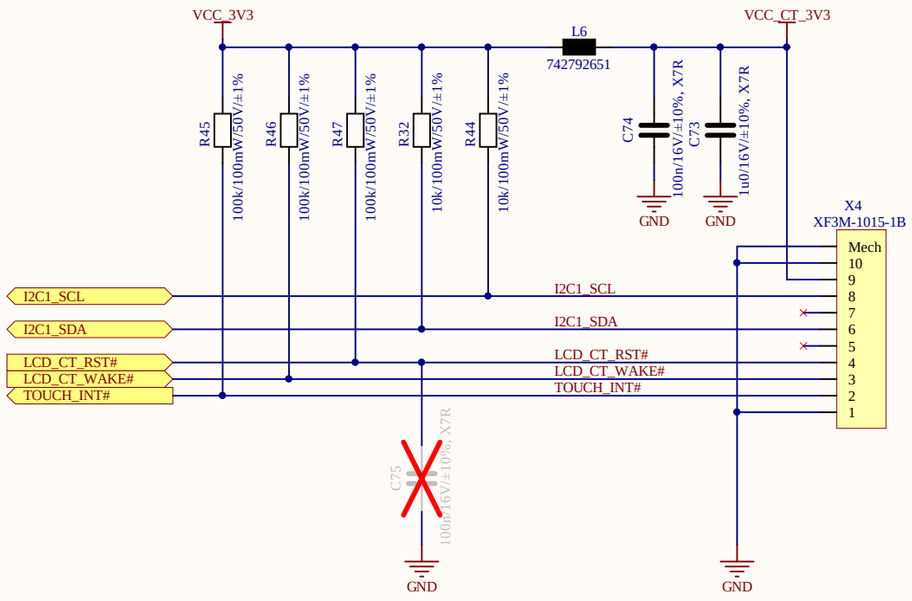
LCD Back Light



Display Connector



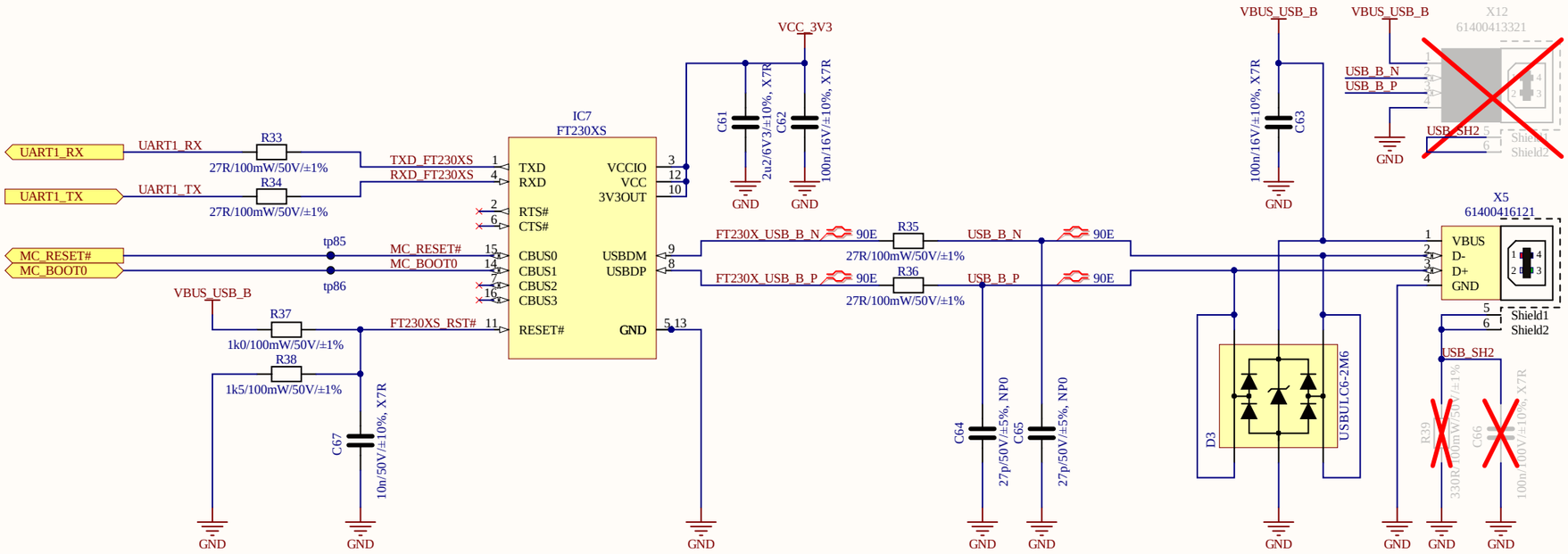
Touch Panel Connector



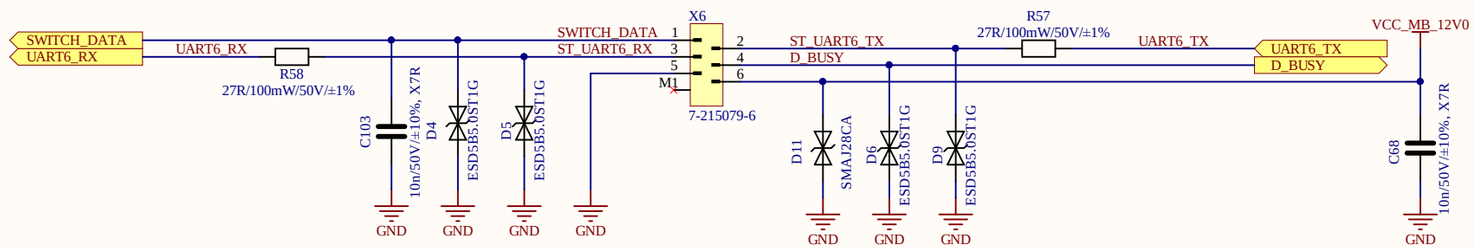
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P09_TFT_Display.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	9

MAIN BOARD INTERFACE

USB Type B Inetrface



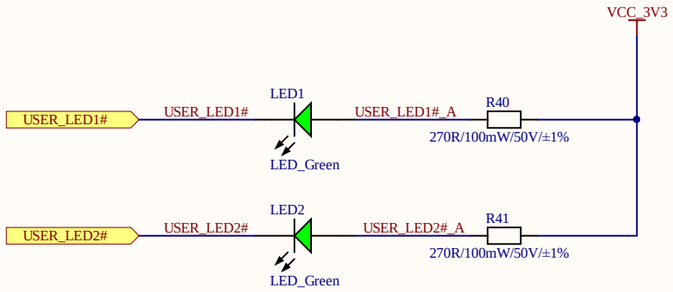
6 pin B2C Connector



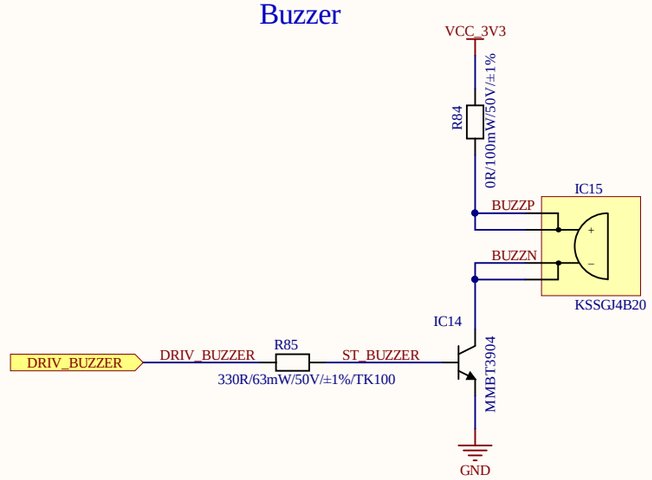
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P10_Main_Board_Interface.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	10

DEBUG AND USER INTERFACE

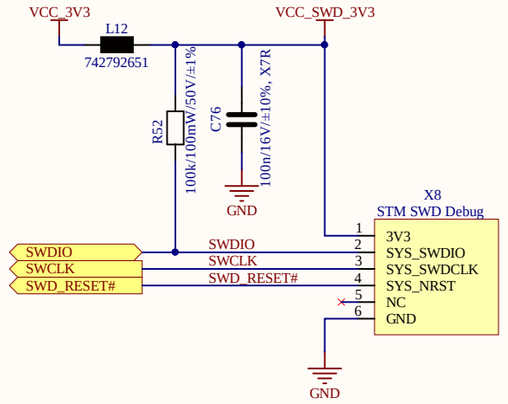
User Interface LED



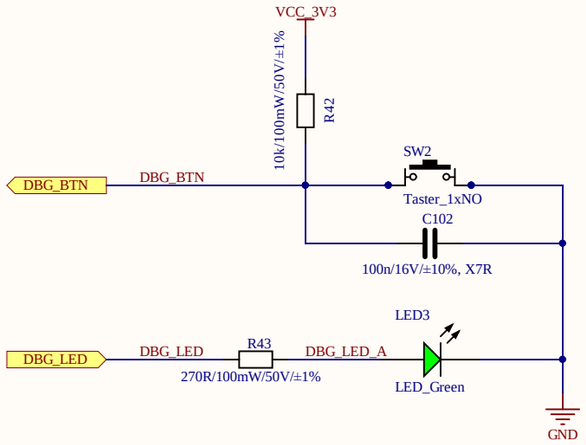
Buzzer



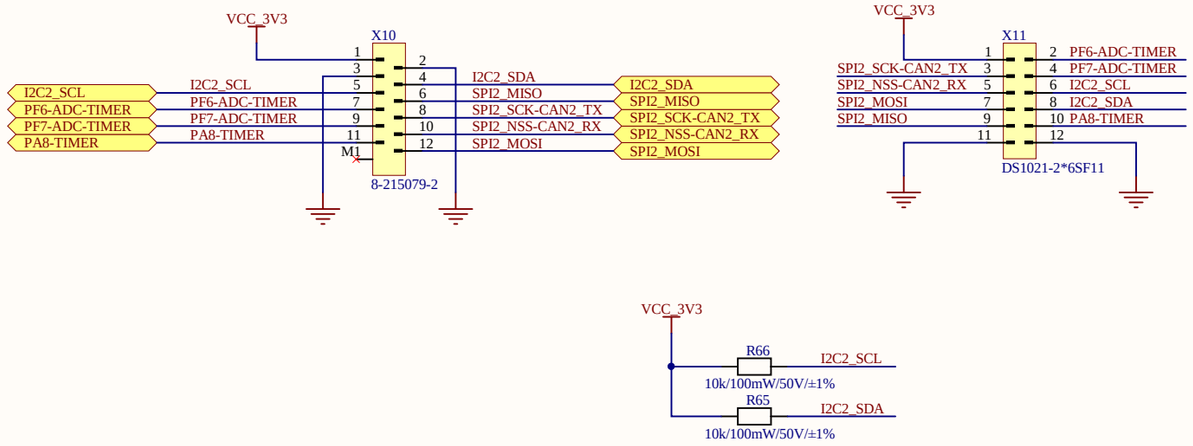
Serial wire Debug Port



Debug Interface

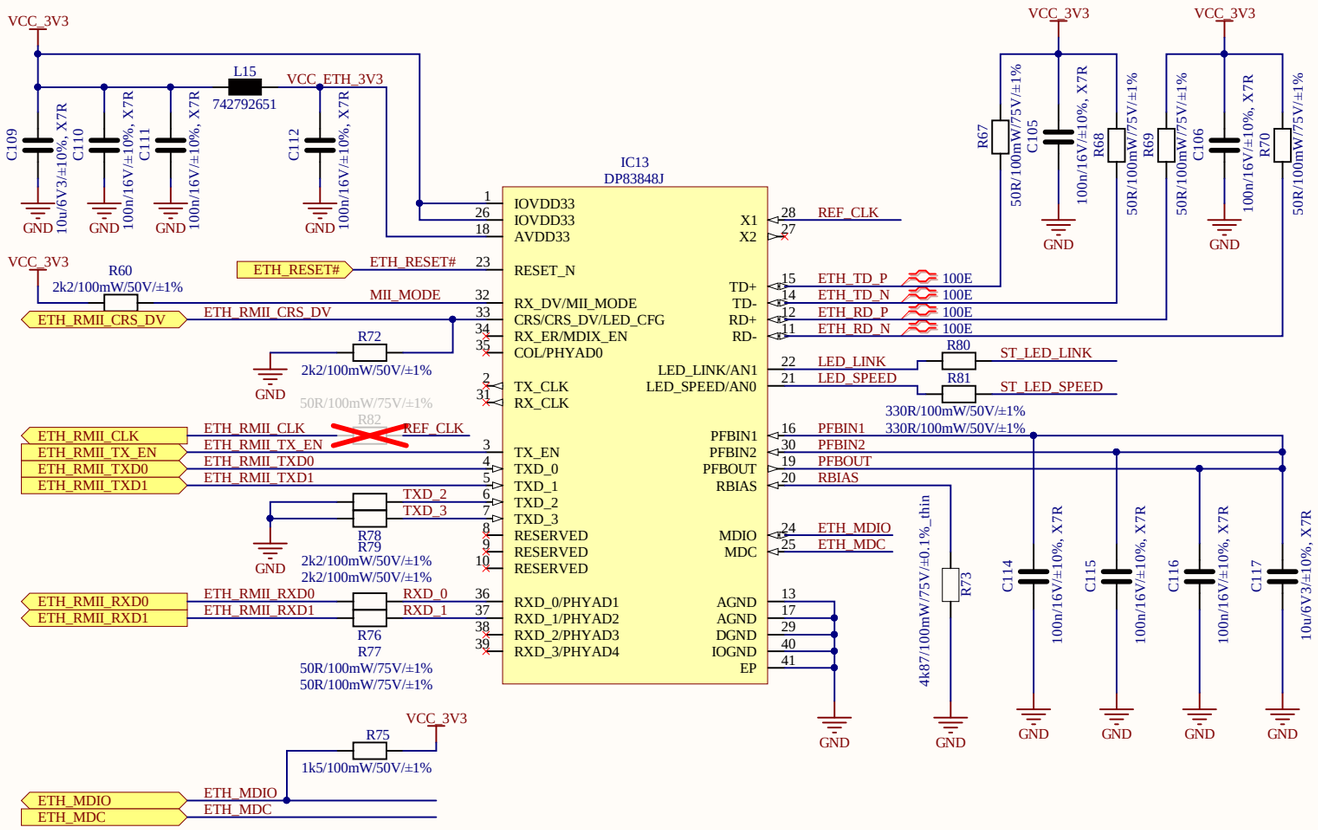


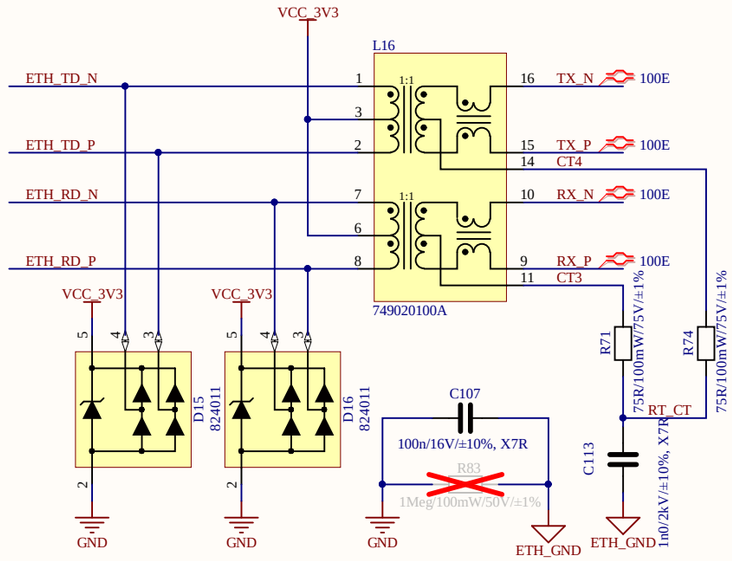
External Interface



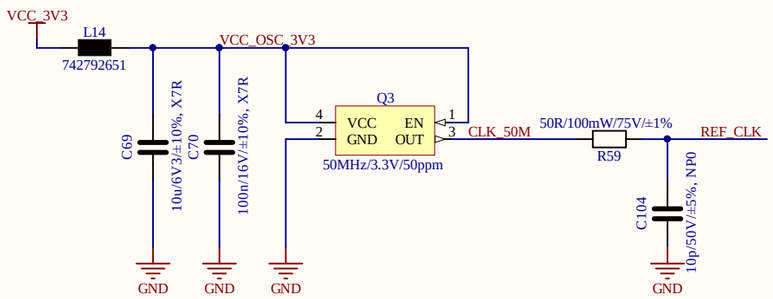
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P11_Debug_And_User_Interface.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	11

ETHERNET INTERFACE

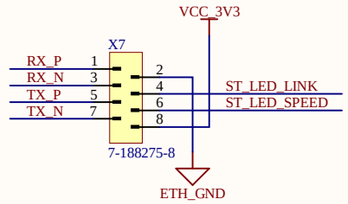




OSCILLATOR



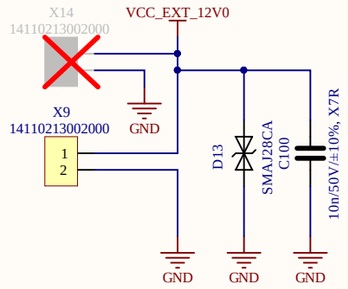
ETHERNET CONNECTOR



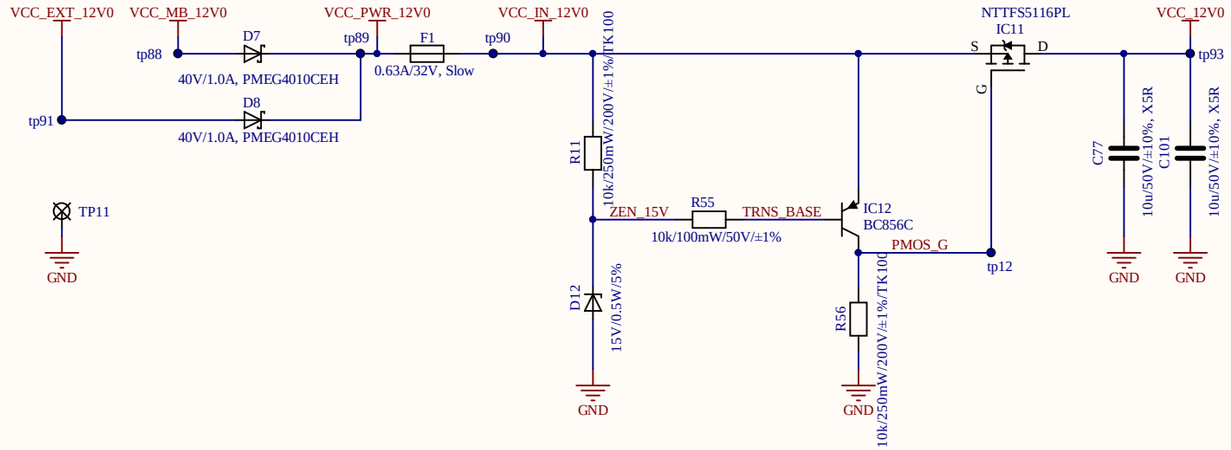
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P12_Ethernet_Interface.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	12

POWER

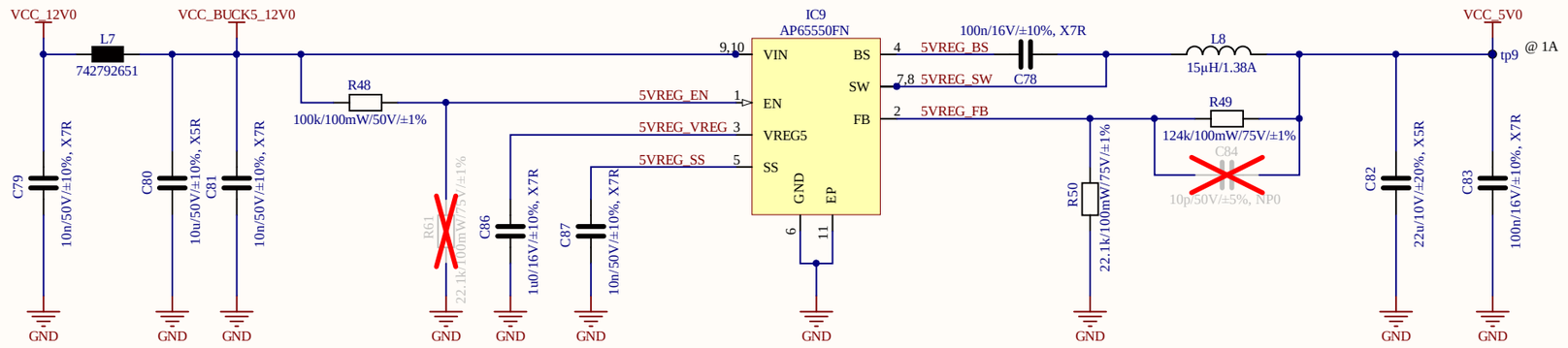
External 12V Power



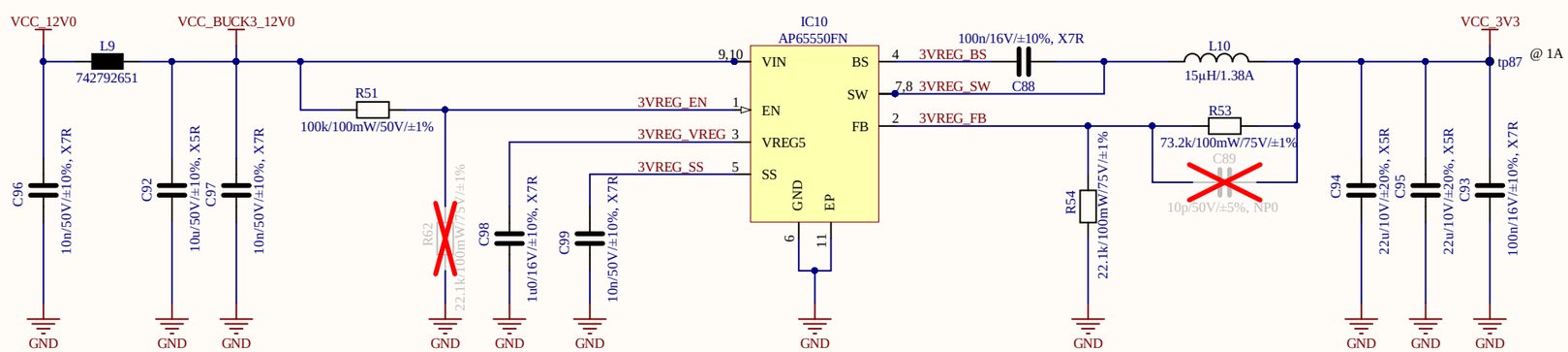
Power Entry



5V Buck Regulator



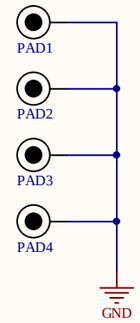
3.3V Buck Regulator



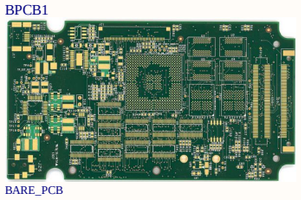
Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project:	Display_Control_Board_V200.PrjPcb		
Document:	P13_Power.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	13

MISCELLANEOUS

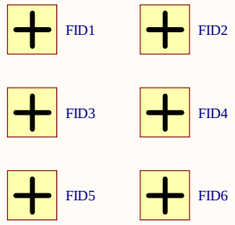
MOUNTING HOLES



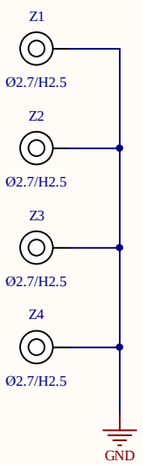
BARE PCB



FIDUCIALS



STEEL SPACER



Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_V200.PrjPcb			
Document:	P14_Miscellaneous.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	14

REVISION HISTORY

Version	Change Description	Change Done By	Approved By	Date
V100	First Release	DCT/VKN	DCT/AVR	03-Apr-2019
V200	1. New connectors (X10, X11) Added 2. HSE Oscillator (Q2, C3, C4, R5) Populated 3. Added pull-up resistor(R64) on SWD_RESET# 4. Added pull-up resistor(R65, R66) to use PB10, PB11 as I2C2 5. USB VBUS Detection (R59, R60) option Deleted 6. Debug Connector (X7) Deleted 7. Ethernet Interface added 8. Buzzer added 9. Mounting Hole size updated 10. Steel spacer added	DCT/VKN	DCT/AVR	01-Jul-2019

Schematics		EBS SYSTART ENTWICKLUNG UND PRODUKTION	
Project: Display_Control_Board_V200.PrjPcb			
Document:	P15_Revision_History.SchDoc	www.ebs-systart.com	
Author:	DCT/VKN	Date:	01-Aug-2019
Auditor:	DCT/AVR	Date:	01-Aug-2019
Status:	Approved	Page:	15